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EXAMINER	
YIGDALL, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2192	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,813	SPRUNT ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,7-9,18,20,21 and 27-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,7-9,18,20,21 and 27-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 7, 2005 has been entered. Claims 1, 3, 4, 7-9, 18, 20, 21 and 27-45 are pending.

Response to Arguments

2. Applicant's arguments have been fully considered but they are not persuasive.

Applicant contends that "Larsen does not disclose or suggest an event selection control register to instruct a multiplexer to select a class of events from a group of event signals issued from the processor and select an event from the class of events by qualifying the event based on a thread ID and a thread CPL" (Applicant's remarks, page 9, last paragraph to page 10, top). Similarly, Applicant contends that "Dreyer does not disclose or suggest an event selection control register to instruct a multiplexer to select a class of events from a group of event signals issued from the processor and select an event from the class of events by qualifying the event based on a thread ID and a thread CPL" (Applicant's remarks, page 10, second paragraph), and similarly again, "nor does Diepstraten disclose or suggest such a feature" (Applicant's remarks, page 11, first paragraph).

However, Applicant is reminded that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re*

Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981), and *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Moreover, Larsen discloses an event selection control register (see, for example, control registers 80 in FIG. 2) to instruct a multiplexer (see, for example, multiplexer 82 in FIG. 2) to select a class of events from a group of event signals (see, for example, the partitions or classes of events in FIG. 2) issued from the processor (see, for example, processor 10 in FIG. 1) and select an event from the class of events (see, for example, column 5, lines 30-36) by qualifying the event based on a thread ID (see, for example, column 5, lines 27-30).

Dreyer similarly discloses an event selection control register (see, for example, control and event select register 17 in FIG. 1) to instruct a multiplexer (see, for example, MUX 22 in FIG. 1) to select an event by qualifying the event based on a thread CPL (see, for example, column 4, lines 39-46).

Therefore, Larsen in view of Dreyer teaches an event selection control register to instruct a multiplexer to select a class of events from a group of event signals issued from the processor and select an event from the class of events by qualifying the event based on a thread ID and a thread CPL.

More specifically, Applicant "can find no disclosure or suggestion in Larsen of selecting a class of events from a group of event signals" and contends that "Larsen does not disclose or suggest further selecting an event by qualifying the event based on a thread ID and a thread CPL" (Applicant's remarks, page 10, first paragraph).

However, in addition to the above, Larsen further discloses that "an event occurrence is handled in a manner dependent upon the event group to which the event occurrence belongs"

(column 5, lines 41-43). An event group is a class of events. "The bit fields within the control registers 80 specify not only the event occurrences, if any, each of PMCs 84 records, but also the mode in which the performance monitor 50 operates (i.e., global or multithreaded) and when counting is enabled and disabled for each of PMCs 84" (column 5, lines 13-17). In particular, FIG. 4 illustrates how a class of events is selected (block 176 for IU/FX/FP events, block 184 for SC events, and block 192 for BIU/LB/L2 events), and how an event is then qualified based on a thread ID (blocks 178 and 186). Larsen lists which events belong to the first class of events (see, for example, column 5, lines 47-56), the second class of events (see, for example, column 5, lines 61-65), and the third class of events (see, for example, column 6, lines 3-9). Here, the thread ID is "thread 0" or "thread 1" (see, for example, column 5, lines 27-30).

Thus, Larsen discloses selecting a class of events from a group of event signals and selecting an event by qualifying the event based on a thread ID. Furthermore, as noted above, Dreyer discloses qualifying an event based on a thread CPL (see, for example, column 4, lines 39-46). Therefore, Larsen in view of Dreyer teaches selecting a class of events from a group of event signals and further selecting an event by qualifying the event based on a thread ID and a thread CPL.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 3, 4, 7-9, 18, 20, 21 and 27-45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

With respect to claim 1, the claim recites "the multiplexer" in lines 6 and 15. There is insufficient antecedent basis for this limitation in the claim. Furthermore, "ECSR" was perhaps intended to read --ESCR-- instead.

With respect to claim 4, the claim recites that the ESCR "further comprises a second field of bits." However, there is no "first field of bits" recited in the claim or its base claim (claim 1) to provide antecedent basis for this limitation. Furthermore, the claim recites "the event to be masked and not counted." There is insufficient antecedent basis for this limitation in the claim.

With respect to claim 18, the claim recites the steps of "instructing a multiplexer to select a class of events from a group of event signals" and then "instructing the multiplexer to select a class of events from the class of event signals." It is not clear whether the second step is redundant or whether it was intended to read --instructing the multiplexer to select an event from the class of events-- instead. There is insufficient antecedent basis for "the class of event signals" in the claim.

With respect to claim 31, the claim recites "an event counter to count the event qualified by the multiplexer." However, its base claim (claim 1) already recites "an event counter to count the event qualified by the multiplexer." It is not clear whether the limitation in claim 31 is redundant or whether it was intended to introduce a second event counter.

With respect to claim 32, the claim recites "the multiplexer" in lines 7 and 17. There is insufficient antecedent basis for this limitation in the claim.

With respect to claim 35, the claim recites "the event to be masked and not counted." There is insufficient antecedent basis for this limitation in the claim.

With respect to claim 40, the claim recites that the machine is to "instruct a multiplexer to select a class of events from a group of event signals" and then "instruct the multiplexer to select a class of events from the class of event signals." It is not clear whether the second step is redundant or whether it was intended to read --instruct the multiplexer to select an event from the class of events-- instead. There is insufficient antecedent basis for "the class of event signals" in the claim.

With respect to claims 3, 7-9, 20, 21, 27-30, 33, 34, 36-39 and 41-45, the claims are dependent upon indefinite base claims and are therefore indefinite for at least the same reasons.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3, 7-9, 18, 20, 21, 27-34 and 36-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,835,705 to Larsen et al. (art of record, "Larsen") in view of U.S. Pat. No. 5,657,253 to Dreyer et al. (art of record, "Dreyer").

With respect to claim 1 (currently amended), Larsen discloses an apparatus comprising:

(a) a processor to execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event (see, for example, processor 10 in FIG. 1, and column 3, lines 39-55, which shows that the multithreaded processor simultaneously executes at least two threads, i.e. a plurality of threads, each comprising a group of instructions, and see, for example, column 6, lines 58-61, which shows that the threads result in events);

(b) an event selection control register (ECSR) to instruct the multiplexer (see, for example, control registers 80 and multiplexer 82 in FIG. 2) to:

(i) select a class of events from a group of event signals issued from the processor (see, for example, column 5, lines 9-17, which shows that the control registers instruct the multiplexer to select events, and see, for example, blocks 176, 184 and 192 in FIG. 4, and column 5, lines 41-43, which shows selecting a group or class of events from the event signals of the processor); and

(ii) select an event from the class of events by qualifying the event based on a thread ID, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred (see, for example, blocks 178 and 186 in FIG. 4, and column 6, line 54 to column 7, line 3, which shows selecting an event from the class of events based on the identity of the thread to which the event corresponds, i.e.

the thread ID of the source thread of the plurality of threads where the event occurred, such as "thread 0" or "thread 1").

Although Larsen discloses qualifying the event based on a thread ID, Larsen does not expressly disclose qualifying the event based on a thread current privilege level (CPL).

However, Dreyer similarly discloses an event selection control register to instruct a multiplexer (see, for example, control and event select register 17 and MUX 22 in FIG. 1) to select an event by qualifying the event based on a thread current privilege level (CPL) (see, for example, column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the apparatus of Larsen with the thread CPL feature taught by Dreyer, so as to differentiate and qualify events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larson also discloses:

(c) an event counter to count the event qualified by the multiplexer (see, for example, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows that the counters record or count the events qualified by the multiplexer).

With respect to claim 3 (currently amended), the rejection of claim 1 is incorporated, and Larsen also discloses the limitation wherein the ESCR comprises a first field of bits to choose the event to be counted (see, for example, column 5, lines 7-17, which shows that the control registers have bit fields to select the events to be counted).

With respect to claim 7 (previously presented), the rejection of claim 1 is incorporated, and although Larsen discloses software-writable event counters (see, for example, column 4, lines 50-57), Larsen does not expressly disclose the limitation wherein the event counter is stopped and cleared before a new event is selected.

However, Dreyer further discloses resetting, i.e. stopping and clearing, the event counter with a software instruction (see, for example, column 3, lines 19-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the counter reset feature taught by Dreyer, so as to stop and clear the counter values in software.

With respect to claim 8 (previously presented), the rejection of claim 7 is incorporated, and although Larsen discloses software-writable event counters (see, for example, column 4, lines 50-57), Larsen does not expressly disclose the limitation wherein the event counter is preset to a certain state.

However, Dreyer further discloses presetting the event counter to a certain value or state (see, for example, column 3, lines 19-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the counter preset feature taught by Dreyer, so as to enable functions such as countdowns (see, for example, Dreyer, column 4, lines 21-30).

With respect to claim 9 (currently amended), the rejection of claim 1 is incorporated, and Larsen also discloses the limitation wherein the class of events includes hardware performance and breakpoint events (see, for example, column 5, lines 47-56, which shows a class of events

that includes hardware performance events such as instructions completed and processor cycles, and breakpoint events such as thread switch counts).

With respect to claim 18 (currently amended), Larsen discloses a method comprising:

(a) executing a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event (see, for example, processor 10 in FIG. 1, and column 3, lines 39-55, which shows that the multithreaded processor simultaneously executes at least two threads, i.e. a plurality of threads, each comprising a group of instructions, and see, for example, column 6, lines 58-61, which shows that the threads result in events);

(b) instructing a multiplexer to select a class of events from a group of event signals issued from the processor (see, for example, multiplexer 82 in FIG. 2, and column 5, lines 9-17, which shows instructing the multiplexer to select events, and see, for example, blocks 176, 184 and 192 in FIG. 4, and column 5, lines 41-43, which shows selecting a group or class of events from the event signals of the processor);

(c) instructing the multiplexer to select a class of events from the class of event signals by qualifying the event based on a thread ID, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred (see, for example, blocks 178 and 186 in FIG. 4, and column 6, line 54 to column 7, line 3, which shows selecting an event from the class of events based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred, such as "thread 0" or "thread 1").

Although Larsen discloses qualifying the event based on a thread ID, Larsen does not expressly disclose qualifying the event based on a thread current privilege level (CPL).

However, Dreyer similarly discloses instructing a multiplexer (see, for example, control and event select register 17 and MUX 22 in FIG. 1) to select an event by qualifying the event based on a thread current privilege level (CPL) (see, for example, column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the method of Larsen with the thread CPL feature taught by Dreyer, so as to differentiate and qualify events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larsen also discloses:

(d) counting the event qualified by the multiplexer using an event counter (see, for example, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows that the counters record or count the events qualified by the multiplexer); and

(e) accessing the event counter to determine a current count of the event (see, for example, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 20 (currently amended), the rejection of claim 18 is incorporated, and Larsen also discloses the limitation wherein the qualifying the event includes requiring that the event has a preselected thread ID (see, for example, column 5, lines 27-30, which shows requiring that the event has a preselected thread ID such as "thread 0" or "thread 1").

With respect to claim 21 (currently amended), the rejection of claim 20 is incorporated, and Dreyer further discloses the limitation wherein the qualifying of the event further includes

requiring that the event has a preselected thread CPL (see, for example, column 4, lines 49-58, which shows requiring that the event has a preselected thread CPL).

With respect to claim 27 (previously presented), the rejection of claim 18 is incorporated, and Dreyer further discloses the limitation wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred (see, for example, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 28 (previously presented), the rejection of claim 20 is incorporated, and Larsen also discloses the limitation wherein the preselected thread ID represents a thread of the plurality of threads where the event occurred (see, for example, column 6, line 54 to column 7, line 3, which shows that the thread ID represents the thread where the event occurred).

With respect to claim 29 (previously presented), the rejection of claim 21 is incorporated, and Dreyer further discloses the limitation wherein thread CPL indicates a privilege level at which the thread was operating at when the event occurred (see, for example, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 30 (previously presented), the rejection of claim 1 is incorporated, and Dreyer further discloses the limitation wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred (see, for

example, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 31 (previously presented), the rejection of claim 1 is incorporated, and further, Larsen also discloses:

(a) an event counter to count the event qualified by the multiplexer (see, for example, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows that the counters record or count the events qualified by the multiplexer); and

(b) an access location to allow access to the event counter to determine a current count of the event (see, for example, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 32 (currently amended), Larsen discloses a system comprising:

(a) a storage medium coupled with a processor (see, for example, main memory 52 and processor 10 in FIG. 1), the processor to execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event (see, for example, column 3, lines 39-55, which shows that the multithreaded processor simultaneously executes at least two threads, i.e. a plurality of threads, each comprising a group of instructions, and see, for example, column 6, lines 58-61, which shows that the threads result in events);

(b) an event selection control register (ESCR) to instruct the multiplexer (see, for example, control registers 80 and multiplexer 82 in FIG. 2) to:

(i) select a class of events from a group of event signals issued from the processor (see, for example, column 5, lines 9-17, which shows that the control registers instruct the multiplexer to select events, and see, for example, blocks 176, 184 and 192 in FIG. 4, and column 5, lines 41-43, which shows selecting a group or class of events from the event signals of the processor); and

(ii) select an event from the class of events by qualifying the event that is to be selected based on a thread ID, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred (see, for example, blocks 178 and 186 in FIG. 4, and column 6, line 54 to column 7, line 3, which shows selecting an event from the class of events based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred, such as "thread 0" or "thread 1").

Although Larsen discloses qualifying the event based on a thread ID, Larsen does not expressly disclose qualifying the event based on a thread current privilege level (CPL).

However, Dreyer similarly discloses an event selection control register to instruct a multiplexer (see, for example, control and event select register 17 and MUX 22 in FIG. 1) to select an event by qualifying the event based on a thread current privilege level (CPL) (see, for example, column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the thread CPL feature taught by Dreyer, so as to differentiate and qualify events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larson also discloses:

(c) an event counter to count the event qualified by the multiplexer (see, for example, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows that the counters record or count the events qualified by the multiplexer); and

(d) an access location to allow access to the event counter to determine a current count of the event (see, for example, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 33 (previously presented), the rejection of claim 32 is incorporated, and Larsen also discloses the limitation wherein the access location allows access to determine the count without disturbing the operation of event counter (see, for example, column 7, lines 40-52, which shows accessing the registers to read the count without disturbing the operation of the counters).

With respect to claim 34 (currently amended), the rejection of claim 33 is incorporated, and the limitations recited in the claim are analogous to those of claim 3 (see the rejection of claim 3 above).

With respect to claim 36 (previously presented), the rejection of claim 32 is incorporated, and the limitations recited in the claim are analogous to those of claim 7 (see the rejection of claim 7 above).

With respect to claim 37 (previously presented), the rejection of claim 36 is incorporated, and the limitations recited in the claim are analogous to those of claim 8 (see the rejection of claim 8 above).

With respect to claim 38 (currently amended), the rejection of claim 32 is incorporated, and the limitations recited in the claim are analogous to those of claim 9 (see the rejection of claim 9 above).

With respect to claim 39 (previously presented), the rejection of claim 32 is incorporated, and the limitations recited in the claim are analogous to those of claim 30 (see the rejection of claim 30 above).

With respect to claim 40 (currently amended), Larsen discloses a machine-readable medium having stored thereon data representing sets of instructions (see, for example, column 3, lines 11-19, which shows a machine-readable medium having instructions stored thereon), the sets of instructions which, when executed by a machine (see, for example, column 4, lines 25-28, which shows executing the instructions), cause the machine to:

(a) execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event (see, for example, processor 10 in FIG. 1, and column 3, lines 39-55, which shows that the multithreaded processor simultaneously executes at least two threads, i.e. a plurality of threads, each comprising a group of instructions, and see, for example, column 6, lines 58-61, which shows that the threads result in events);

(b) instruct a multiplexer to select a class of events from a group of event signals issued from the processor (see, for example, multiplexer 82 in FIG. 2, and column 5, lines 9-17, which

shows instructing the multiplexer to select events, and see, for example, blocks 176, 184 and 192 in FIG. 4, and column 5, lines 41-43, which shows selecting a group or class of events from the event signals of the processor);

(c) instruct the multiplexer to select a class of events from the class of event signals by qualifying the event based on a thread ID, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred (see, for example, blocks 178 and 186 in FIG. 4, and column 6, line 54 to column 7, line 3, which shows selecting an event from the class of events based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred, such as "thread 0" or "thread 1").

Although Larsen discloses qualifying the event based on a thread ID, Larsen does not expressly disclose qualifying the event based on a thread current privilege level (CPL).

However, Dreyer similarly discloses instructing a multiplexer (see, for example, control and event select register 17 and MUX 22 in FIG. 1) to select an event by qualifying the event based on a thread current privilege level (CPL) (see, for example, column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the machine-readable medium of Larsen with the thread CPL feature taught by Dreyer, so as to differentiate and qualify events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larsen also discloses:

(d) count the event qualified by the multiplexer using an event counter (see, for example, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows that the counters record or count the events qualified by the multiplexer); and

(e) access the event counter to determine a current count of the event (see, for example, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 41 (previously presented), the rejection of claim 40 is incorporated, and the limitations recited in the claim are analogous to those of claim 20 (see the rejection of claim 20 above).

With respect to claim 42 (previously presented), the rejection of claim 41 is incorporated, and the limitations recited in the claim are analogous to those of claim 21 (see the rejection of claim 21 above).

With respect to claim 43 (previously presented), the rejection of claim 40 is incorporated, and the limitations recited in the claim are analogous to those of claim 27 (see the rejection of claim 27 above).

With respect to claim 44 (previously presented), the rejection of claim 40 is incorporated, and the limitations recited in the claim are analogous to those of claim 28 (see the rejection of claim 28 above).

With respect to claim 45 (previously presented), the rejection of claim 41 is incorporated, and the limitations recited in the claim are analogous to those of claim 29 (see the rejection of claim 29 above).

7. Claims 4 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen in view of Dreyer, as applied to claims 1 and 34 above, respectively, and further in view of U.S. Pat. No. 6,205,468 to Diepstraten et al. (art of record, "Diepstraten").

With respect to claim 4 (currently amended), the rejection of claim 1 is incorporated, and although Larsen discloses that the control registers have bit fields to select the events to be recorded, set the mode of operation, and enable or disable event counting (see, for example, column 5, lines 7-17), Larsen does not expressly disclose the limitation wherein the ESCR further comprises a second field of bits to choose the event to be masked and not counted.

However, Diepstraten discloses an event masker associated with an event recorder that includes control bits for masking events (see, for example, event mask register 90 in FIG. 3, and column 4, lines 42-50, which shows masking events to select one or more events to be ignored, i.e. not counted).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the apparatus of Larsen with the event masking feature taught by Diepstraten, so as to reduce the number of events that will be processed (see, for example, Diepstraten, column 4, lines 42-50).

With respect to claim 35 (currently amended), the rejection of claim 34 is incorporated, and the limitations recited in the claim are analogous to those of claim 4 (see the rejection of claim 4 above).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. U.S. Pat. No. 6,356,615 to Coon et al. discloses a programmable event counter system. U.S. Pat. No. 6,112,318 to Jouppi et al. discloses performance counters controlled by programmable logic. U.S. Pat. No. 5,796,637 to Glew et al. discloses an apparatus and method for filtering event signals.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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